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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,298	04/23/2001	Michitaka Urushima	NEC01P030-HSc	3167

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EXAMINER

GEYER, SCOTT B

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 05/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/839,298

Applicant(s)

URUSHIMA, MICHITAKA

Examiner

Scott Geyer

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 April 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 10-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 10-24 are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-9 and 25, drawn to a semiconductor device, classified in class 257, subclass 678+.
- II. Claims 10-24, drawn to a method for making a device, classified in class 438, subclass 106+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the method claims recite etching to remove a portion of the resin to expose the conductive bumps. The device could be made by alternative methods, such as planarization, pre-molding or CMP.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Sean McGinn on 21 March 2001 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-9 and 25. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

***Priority***

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Drawings***

7. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

***Specification***

8. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware of in the specification.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-6 and 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by the applicant's admission of prior art.

As to **claim 1**, applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d).

As to **claim 2**, applicant's prior art figure 3 teaches a chip (70) with bumps (80) to be attached to an interposer (72B).

As to **claim 3**, applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d) and applicant's prior art figure 3 teaches a chip (70) with bumps (80) to be attached to an interposer (72B).

As to **claim 4**, applicant's prior art figure 3 teaches an interposer (72B) with a device hole (96).

As to **claim 5**, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98) on the surface of a chip and allowing bumps (80) to be exposed and electrically attach to a wiring pattern on an interposer (72B). The wiring pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls.

As to **claim 6**, applicant's prior art figure 3 teaches a semiconductor chip (70) with an adhesive layer (98), which can be a resin layer (applicant's disclosure, page 4, lines 3-16) on the surface of a chip and allowing bumps (80) to be exposed and

electrically attach to a wiring pattern on an interposer (72B). The wiring pattern adheres to the adhesive layer. The opposite surface of the interposer has an insulating and covering layer which has openings for external connections (96) such as solder balls.

As to **claim 9**, applicant's prior art figure 2 teaches a protection film (18) which can be a resin layer (applicant's disclosure, page 4, lines 3-16). The disclosure further defines the resin as a layer that which is applied and then cured, which therefor plainly depicts a thermoplastic resin.

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(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

11. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Jackson (6,285,081 B1).

Jackson teaches a semiconductor chip (figure 1B, numeral 115) with an adhesive layer (130) provided on the surface of the chip with solder bumps (125). The solder bumps are exposed through the adhesive layer. A tape substrate (135) is used to connect the die to an interposer whereby the interposer is a circuit board (110). The chip is attached to the "front" side of the tape and the interposer is attached to the "back" side of the tape, and electrical connection is provided between the chip, tape and interposer by solder bumps (125) and (145).

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roldan et al. (6,005,292) in view of applicant's admission of prior art.

Roldan et al. teach a stacked chip arrangement wherein two chips (figure 2C, numerals 30 and 36) are brought together to form a device where the two chips are electrically connected to each other (figure 2D). The electrical connection is made between solder bumps (figure 2C, numerals 34 and 44).

Roldan et al. do not teach an adhesive layer covering a surface of each chip where the solder bumps are exposed through the adhesive layer.

However, the applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Roldan et al. with an adhesive layer as taught by the applicant's admitted prior art. The adhesive layer, incorporated into the device of Roldan et al., would provide an extra means of attachment for the two devices in addition to the re-flowed solder bumps (figure 2D), ensuring a better bond between the

two devices. Also, the adhesive layer would provide protection to the electrical connection from environmental factors such as moisture.

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14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mostafazadeh et al. (5,783,870) in view of applicant's admission of prior art.

Mostafazadeh et al. teach a stacked chip arrangement wherein multiple chips are stacked on top of one another (figure 4A). The chips are bonded using bond pads on the top surfaces and bottom surfaces of the chips and using solder balls to make electrical connections between each chip (see figures 4B and 4C).

Mostafazadeh et al. do not teach an adhesive layer covering a surface of each chip where the solder bumps are exposed through the adhesive layer.

However, the applicant's prior art figure 2 teaches a semiconductor chip (11), a stud bump (13) and an adhesive layer of protection film (18). The stud bumps (13) project from the surface as they are exposed (figure 2d).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the device of Mostafazadeh et al. with an adhesive layer as taught by the applicant's admitted prior art. The adhesive layer, incorporated into the device stack of Mostafazadeh et al., would provide an extra means of attachment for the devices in addition to the solder bumps, ensuring a better bond between the devices. Also, the adhesive layer would provide protection to the electrical connection from environmental factors such as moisture.

**Conclusion**

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: **scott.geyer@uspto.gov**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (703) 308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sbg  
May 6, 2002



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